REMARKS

In the non-final Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 102(e) as anticipated by Zhang et al. (U.S. Patent No. 6,795,506).

Applicants respectfully traverse the Examiner's rejection under 35 U.S.C. § 102. Claims 1-61 remain pending.

Applicants note that the Examiner did not address claims 58-61. Applicants assume that the Examiner intended to identify claims 58-61 as containing allowable subject matter. If Applicants' assumption is incorrect, Applicants respectfully request clarification as to the status of claims 58-61. If the Examiner intended to reject claims 58-61, the Examiner did not address the features of claims 58-61 and, therefore, did not establish a prima facie case to deny patentability of claims 58-61.

In paragraphs 1-23 of the Office Action, the Examiner rejected claims 1-57 under 35 U.S.C. § 102(e) as allegedly anticipated by Zhang et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Zhang et al. does not disclose or suggest the combination of features recited in claims 1-57.

Independent claim 1, for example, is directed to a system for processing data received in a plurality of incoming streams of variable speeds. The system comprises a memory configured to store data associated with a plurality of incoming streams of variable speeds, an interface

controller comprising a first arbitration element to arbitrate among the streams of variable speeds to store the data in the memory, and a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read the data from the memory.

Zhang et al. does not disclose or suggest the combination of features recited in claim 1. For example, Zhang et al. does not disclose or suggest an interface controller comprising a first arbitration element to arbitrate among streams of variable speeds to store the data in a memory.

The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 1). Applicants disagree.

At column 21, line 52 - column 22, line 1, Zhang et al. discloses:

> The rate controller 409 connects to both the bit rate converter apparatus 406 and the scheduler 411 and determines what bit rate is to be used for each input compressed bitstream. More specifically, based on messages received from the rate controller 409, the bit rate converter apparatus 406 adjusts the bit rate for each compressed bitstream. In one embodiment, the objective of the rate controller 409 is to determine whether to apply more aggressive transcoding and bit rate conversion to a particular compressed bitstream and use the saved bandwidth resulting therefrom for a different compressed bitstream. In a statistical re-multiplexing environment for example, if a particular compressed bitstream is encoded with fewer number of bits, then the remaining compressed bitstreams in the multiplex will be able to use more bits, resulting in a quality trade-off between different compressed bitstreams via bandwidth re-allocation.

In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose a memory configured to store data associated with a plurality of incoming streams of variable speeds and, therefore, Zhang et al. cannot disclose or suggest an interface controller comprising a first arbitration element to arbitrate among streams of variable speeds to store data in the memory, as required by claim 1.

The Examiner relied on column 29, lines 49-57, as allegedly disclosing the memory (Office Action, paragraph 1). At column 29, lines 49-57, Zhang et al. discloses:

> Regardless of network device's configuration (for cable plants or otherwise), it may employ one or more memories or memory modules (e.g., memory 861) configured to store program instructions for the network operations and other functions of the present invention described herein. The program instructions may specify an operating system and one or more applications, for example. Such memory or memories may also be configured to store data streams, data structures or other specific non-program information described herein.

In this section, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a memory configured to store data associated with a plurality of incoming streams of variable speeds (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest that bit rate converter apparatus 406, or any of the other elements shown in Fig. 5A, comprises a first arbitration element to arbitrate among streams of variable speeds to store data in the memory, as required by claim 1.

Zhang et al. also does not disclose or suggest a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read data from the memory, as further recited in claim 1. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 1). Applicants respectfully disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose a memory configured to store data associated with a plurality of incoming streams of variable speeds and, therefore, Zhang et al. cannot

disclose or suggest a dispatch unit comprising a second arbitration element to arbitrate among the streams of variable speeds to read data from the memory, as required by claim 1.

As explained above, the Examiner relied on column 29, lines 49-57, as allegedly disclosing the memory (Office Action, paragraph 1). At column 29, lines 49-57, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a memory configured to store data associated with a plurality of incoming streams of variable speeds (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest that bit rate converter apparatus 406, or any of the other elements shown in Fig. 5A, comprises a second arbitration element to arbitrate among the streams of variable speeds to read data from the memory, as required by claim 1.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Zhang et al. Claims 2-20 depend from claim 1 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 1. Claims 2-20 are also not anticipated by Zhang et al. for reasons of their own.

For example, claim 2 recites that the memory includes a plurality of memory buckets corresponding to the streams. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 28, line 65 - column 29, line 3, of Zhang et al. for support (Office Action, paragraph 3). Applicants disagree.

At column 28, line 64 - column 29, line 3, Zhang et al. discloses:

> In an alternative embodiment, processor 863 is specially designed hardware for controlling the operations of router 810. In a preferred embodiment, a memory 861 (such

> as non-volatile RAM and/or ROM) also forms part of CPU 862. However, there are many different ways in which memory could be coupled to the system.

In this section, Zhang et al. discloses that CPU 862 includes a memory 861 that may take the form of non-volatile RAM and/or ROM. Even assuming, for the sake of argument, that memory 861 can be equated to a memory configured to store data associated with a plurality of incoming streams of variable speeds (a point that Applicants do not concede), Zhang et al. does not disclose or remotely suggest that memory 861 includes a plurality of memory buckets corresponding to a plurality of streams of variable speeds, as required by claim 2.

For at least these additional reasons, Applicants submit that claim 2 is not anticipated by Zhang et al. Claim 3 depends from claim 2 and is, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 2.

Claim 4 recites that the first arbitration element is configured to store a plurality of entries, each of the entries including a stream number that identifies one of the streams. Zhang et al. does not disclose or suggest these features. The Examiner alleged that Zhang et al. discloses these features and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 5). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or remotely suggest a first arbitration element that arbitrates among streams of variable speeds to store data in a memory, where the first arbitration element is configured to store a plurality of entries, each of the entries including a stream number that identifies one of the streams, as required by claim 4.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Zhang et al. Claims 5-8 depend from claim 4 and are, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 4.

Claim 9 recites that the first and second arbitration elements are synchronized. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 19, lines 41-54, of Zhang et al. for support (Office Action, paragraph 10). Applicants disagree.

At column 19, lines 41-55, Zhang et al. discloses:

> In order to effectively extract and use the bit rate information, it is synchronized with a compressed elementary stream by the encoding multiplexer, e.g. the scheduler 66 of FIG. 3C in a timely manner. In one embodiment, the bit rate information is inserted prior to the start of the access unit it is associated with More specifically, it is inserted just before the picture_start_code of the associated access unit, but not before the picture_start_code of the previous access_unit.
>
> FIG. 4C illustrates the insertion of a transport packet 360 containing the bit rate information 302a into a transport stream 362 according to one embodiment of the present invention. The transport stream 362 includes three transport packets 364, 366 and 368 that contain packetized data from access unit (N-1) 370 and access unit (N) 372.

In this section, Zhang et al. discloses that the encoding multiplexer (e.g., scheduler 66) synchronizes the bit rate information with a compressed elementary stream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest a first arbitration element (to arbitrate among the streams of variable speeds to store data in a memory) or a second arbitration element (to arbitrate among the streams of variable speeds to read data from a memory), let alone first and second arbitration elements that are synchronized, as required by claim 9. Synchronization of bit rate information with a compressed elementary stream cannot reasonably be equated to first and second arbitration elements that are synchronized, as required by claim 9.

For at least these additional reasons, Applicants submit that claim 9 is not anticipated by Zhang et al.

Claim 10 recites that the second arbitration element is configured to store a plurality of entries, each of the entries including a stream number that identifies one of the streams. Zhang et al. does not disclose or suggest these features. The Examiner alleged that Zhang et al. discloses these features and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 11). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or remotely suggest a second arbitration element that arbitrates among streams of variable speeds to read data from a memory, where the second arbitration element is configured to store a plurality of entries, each of the entries including a stream number that identifies one of the streams, as required by claim 10.

For at least these additional reasons, Applicants submit that claim 10 is not anticipated by Zhang et al. Claims 11 and 12 depend from claim 10 and are, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 10.

Claim 13 recites flow control logic configured to initiate flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 14). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose a memory configured to store data associated with a plurality of incoming streams of variable speeds and, therefore, Zhang et al. cannot disclose or suggest flow control logic configured to initiate flow control on the storing of data in the memory, as required by claim 13.

As explained above, the Examiner relied on column 29, lines 49-57, as allegedly disclosing the memory (Office Action, paragraph 1). At column 29, lines 49-57, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a memory configured to store data associated with a plurality of incoming streams of variable speeds (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest that bit rate converter apparatus 406, or any of the other elements shown in Fig. 5A, is configured to initiate flow control on the storing of data in the memory, as required by claim 13.

For at least these additional reasons, Applicants submit that claim 13 is not anticipated by Zhang et al. Claims 14-18 depend from claim 13 and are, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 13.

Claim 19 recites that each of the streams has an associated watermark for use in performing flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited

column 21, lines 45-51, of Zhang et al. for support (Office Action, paragraph 20). Applicants disagree.

At column 21, lines 45-51, Zhang et al. discloses:

> The multiplexer 408 also includes the rate controller 409 and a set of multiple input buffers 407. The input buffers 407 temporarily store compressed video data received from the transcoder 406 for each of the input compressed bitstreams until the scheduler 411 processes the compressed video data for transmission. In one embodiment, the multiplexer 408 is an open loop multiplexer.

In this section, Zhang et al. discloses input buffers that temporarily store compressed video data for each of the input compressed bitstreams until scheduler 411 processes the compressed video data for transmission. Nowhere in this section does Zhang et al. disclose or suggest each of a plurality of streams that has an associated watermark for use in performing flow control on the storing of data in memory, as required by claim 19.

For at least these additional reasons, Applicants submit that claim 19 is not anticipated by Zhang et al.

Claim 20 recites that each of the streams has two associated watermarks for use in performing flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 45-51, of Zhang et al. for support (Office Action, paragraph 21). Applicants disagree.

Column 21, lines 45-51, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses input buffers that temporarily store compressed video data for each of the input compressed bitstreams until scheduler 411 processes the compressed video data for transmission. Nowhere in this section does Zhang et al. disclose or suggest each of a plurality of streams that

has two associated watermarks for use in performing flow control on the storing of data in memory, as required by claim 20.

For at least these additional reasons, Applicants submit that claim 20 is not anticipated by Zhang et al.

Independent claim 21 is directed to a method for processing data received in a plurality of incoming streams of variable speeds. The method comprises storing data from a plurality of variable speed streams in a memory using a first arbitration element that arbitrates among the variable speed streams, and reading the data from the memory using a second arbitration element that arbitrates among the variable speed streams.

Zhang et al. does not disclose or suggest the combination of features recited in claim 21. For at least reasons similar to reasons given with regard to claim 1, Zhang et al. does not disclose or suggest storing data from a plurality of variable speed streams in a memory using a first arbitration element that arbitrates among the variable speed streams, or reading the data from the memory using a second arbitration element that arbitrates among the variable speed streams.

For at least these reasons, Applicants submit that claim 21 is not anticipated by Zhang et al. Claims 22-39 depend from claim 21 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 21. Claims 22-39 also recite features similar to, but possibly different in scope from, features recited in claims 2-20. Claims 22-39 are, therefore, also not anticipated by Zhang et al. for at least reasons similar to reasons given with regard to claims 2-20.

Independent claim 40 is directed to a system for performing flow control on data in a plurality of incoming streams of variable speeds. The system comprises a buffer configured to

temporarily store data from a plurality of streams of variable speeds in a plurality of entries, a counter configured to determine a number of entries in the buffer corresponding to each of the streams, and a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream.

Zhang et al. does not disclose or suggest the combination of features recited in claim 40. For example, Zhang et al. does not disclose or suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds. The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting a similar feature in claim 16, however, the Examiner alleged that Zhang et al. discloses a counter that is configured to determine a number of entries in a buffer corresponding to each of the streams and cited column 29, lines 49-57, of Zhang et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 29, lines 49-57, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as required by claim 40.

Zhang et al. also does not disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream, as further recited in claim 40. The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting a similar feature in claim 16, however, the Examiner alleged that Zhang et al. discloses a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 21, lines 52-67, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams of variable speeds based on the determined number of entries for the stream, as required by claim 40.

For at least these reasons, Applicants submit that claim 40 is not anticipated by Zhang et al. Claims 41-47 depend from claim 40 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 40.

Independent claims 48 and 55 recite features similar to, but possibly different in scope from, features recited in claim 40. Claims 48 and 55 are, therefore, not anticipated by Zhang et al. for at least reasons similar to reasons given with regard to claim 40. Claims 49-54 depend

from claim 48 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 48.

Independent claims 56 and 57 recite features similar to, but possibly different in scope from, features recited in claim 1. Claims 56 and 57 are, therefore, not anticipated by Zhang et al. for at least reasons similar to reasons given with regard to claim 1.

In view of the foregoing remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-61.

As Applicants' remarks with respect to the Examiner's rejections are sufficient to overcome these rejections, Applicants' silence as to certain assertions by the Examiner in the Office Action or certain requirements that may be applicable to such rejections (e.g., whether a reference constitutes prior art, motivation to combine references, etc.) is not a concession by Applicants that such assertions are accurate or such requirements have been met, and Applicants reserve the right to analyze and dispute these assertions/requirements in the future.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY SNYDER, LLP

/Paul A. Harrity/
Paul A. Harrity
Reg. No. 39,574

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11350 Random Hills Road
Suite 600
Fairfax, Virginia 22030
(571) 432-0800